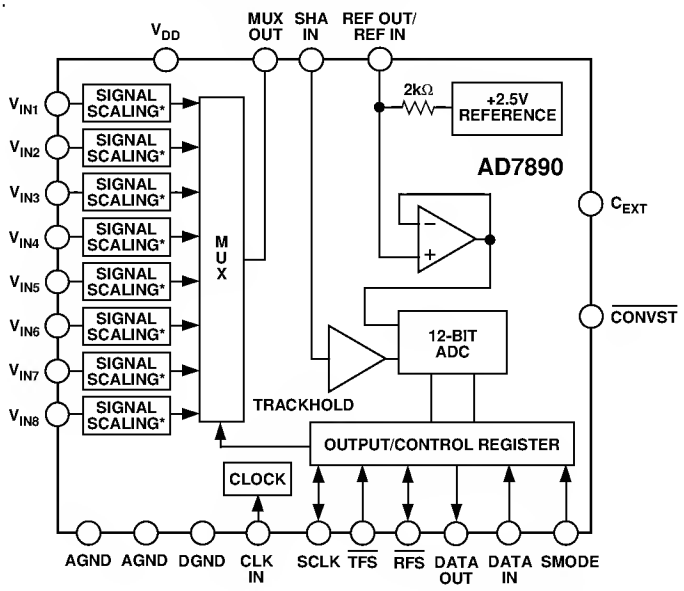
LC²MOS 8-Channel, 12-Bit Serial, Data Acquisition System

AD7890

FEATURES

Fast 12-Bit ADC with 5.9 μs Conversion Time
Eight Single-Ended Analog Input Channels
Selection of Input Ranges:
±10 V for AD7890-10
0 V to +4.096 V for AD7890-4
0 V to +2.5 V for AD7890-2
Allows Separate Access to Multiplexer and ADC
On-Chip Track/Hold Amplifier
On-Chip Reference
High Speed, Flexible, Serial Interface
Single Supply, Low Power Operation (50 mW max)
Power-Down Mode (75 μW typ)

FUNCTIONAL BLOCK DIAGRAM



*NO SCALING ON AD7890-2

GENERAL DESCRIPTION

The AD7890 is an eight-channel 12-bit data acquisition system. The part contains an input multiplexer, an on-chip track/hold amplifier, a high-speed 12-bit ADC, a +2.5 V reference and a high speed, serial interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2).

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter or signal conditioning, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in the filter or signal conditioning circuitry.

Output data from the AD7890 is provided via a high speed bidirectional serial interface port. The part contains an on-chip control register, allowing control of channel selection, conversion start and power-down via the serial port. Versatile, high speed logic ensures easy interfacing to serial ports on microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7890 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is low at 30 mW typ and the part can be placed in a standby (power-down) mode if it is not required to perform conversions. The AD7890 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

PRODUCT HIGHLIGHTS

1. Complete 12-Bit Data Acquisition System on a Chip
   The AD7890 is a complete monolithic ADC combining an eight-channel multiplexer, 12-bit ADC, +2.5 V reference and a track/hold amplifier on a single chip.
2. Separate Access to Multiplexer and ADC
   The AD7890 provides access to the output of the multiplexer allowing one antialiasing filter for eight channels—a considerable saving over the eight antialiasing filters required if the multiplexer was internally connected to the ADC.
3. High Speed Serial Interface
   The part provides a high speed serial interface for easy connection to serial ports of microcontrollers and DSP processors.

REV. A

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AD7890–SPECIFICATIONS (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, $f_{CLK\,IN}$ = 2.5 MHz external, MUX OUT connect to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Using External $\overline{CONVST}$. Any Channel
Signal to (Noise + Distortion) Ratio[2]	70	70	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Total Harmonic Distortion (THD)[2]	–78	–78	–78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Peak Harmonic or Spurious Noise[2]	–79	–79	–79	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 100 kHz[3]
2nd Order Terms	–80	–80	–80	dB typ	
3rd Order Terms	–80	–80	–80	dB typ	
Channel-to-Channel Isolation[2]	–80	–80	–80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[2]	±1	±0.5	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±2.5	±2.5	±2.5	LSB max	
Full-Scale Error Match[4]	2	2	2	LSB max	
AD7890-2, AD7890-4					
Unipolar Offset Error[2]	±2	±2	±2	LSB max	
Unipolar Offset Error Match	2	2	2	LSB max	
AD7890-10 Only					
Negative Full-Scale Error[2]	±2	±2	±2	LSB max	
Bipolar Zero Error[2]	±4	±4	±4	LSB max	
Bipolar Zero Error Match	2	2	2	LSB max	
ANALOG INPUTS					
AD7890-10					
Input Voltage Range	±10	±10	±10	Volts	
Input Resistance	20	20	20	kΩ min	
AD7890-4					
Input Voltage Range	0 to +4.096	0 to +4.096	0 to +4.096	Volts	
Input Resistance	11	11	11	kΩ min	
AD7890-2					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	200	nA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance					
(AD7890-10, AD7890-4)	3/5	3/5	3/5	kΩ min/kΩ max	
(AD7890-2)	2	2	2	kΩ max	Assuming V_{IN} Is Driven from Low Impedance
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	±50	±50	±50	nA max	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[5]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	2	2	2	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Serial Data Output Coding					
AD7890-10	2s Complement				
AD7890-4	Straight (Natural) Binary				
AD7890-2	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	5.9	5.9	5.9	μs max	$f_{CLK\ IN}$ = 2.5 MHz, MUX OUT Connected to SHA IN
Track/Hold Acquisition Time[2, 5]	2	2	2	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	10	10	10	mA max	Logic Inputs = 0 V or V_{DD}
I_{DD} (Standby Mode)[6] @ +25°C	15	15	15	μA typ	Logic Inputs = 0 V or V_{DD}
Power Dissipation					
Normal Mode	50	50	50	mW max	Typically 30 mW
Standby Mode @ +25°C	75	75	75	μW typ	

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to –85°C; S Version: –55°C to +125°C.
[2]See Terminology.
[3]This sample rate is only achievable when tiling the part in external clocking mode.
[4]Full-scale error match applies to positive full scale for the AD7890-2 and AD7890-4. It applies to both positive and negative full scale for the AD7890-10.
[5]Sample tested @ +25°C to ensure compliance.
[6]Analog inputs on AD7890-10 must be at 0 V to achieve correct power-down current.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
AD7890-10, AD7890-4 ..... ±17 V
AD7890-2 ..... –5 V, +10 V
Reference Input Voltage to AGND ... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) ..... –40°C to +85°C
Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature (Soldering, 10 sec) ..... +260°C
Cerdip Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 70°C/W
Lead Temperature (Soldering, 10 sec) ..... +300°C
SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Linearity Error	Package Option*
AD7890AN-2	–40°C to +85°C	±1 LSB	N-24
AD7890BN-2	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-2	–40°C to +85°C	±1 LSB	R-24
AD7890BR-2	–40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-2	–55°C to +125°C	±1 LSB	Q-24
AD7890AN-4	–40°C to +85°C	±1 LSB	N-24
AD7890BN-4	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-4	–40°C to +85°C	±1 LSB	R-24
AD7890BR-4	–40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-4	–55°C to +125°C	±1 LSB	Q-24
AD7890AN-10	–40°C to +85°C	±1 LSB	N-24
AD7890BN-10	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-10	–40°C to +85°C	±1 LSB	R-24
AD7890BR-10	–40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-10	–55°C to +125°C	±1 LSB	Q-24

NOTE
*N = Plastic DIP; Q = Cerdip; R = SOIC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7890 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V, f_{CLKIN} = 2.5 MHz external, MUX OUT connected to SHA IN.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, B, S Versions)	Units	Conditions/Comments
f_{CLKIN}[3]	100	kHz min	Master Clock Frequency. For Specified Performance
	2.5	MHz max	
$t_{CLK\ IN\ LO}$	0.3 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
$t_{CLK\ IN\ HI}$	0 3 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
tr[4]	25	ns max	Digital Output Rise Time. Typically 10 ns
tf[4]	25	ns max	Digital Output Fall Time. Typically 10 ns
$t_{CONVERT}$	5.9	µs max	Conversion Time
t_{CST}	100	ns min	$\overline{CONVST}$ Pulse Width
Self-Clocking Mode			
t_1	$t_{CLK\ IN\ HI}$ + 50	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_2[5]	25	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_3	$t_{CLK\ IN\ HI}$	ns nom	SCLK High Pulse Width
t_4	$t_{CLK\ IN\ LO}$	ns nom	SCLK Low Pulse Width
t_5[5]	20	ns max	SCLK Rising Edge to Data Valid Delay
t_6	40	ns max	SCLK Rising Edge to $\overline{RFS}$ Delay
t_7[6]	50	ns max	Bus Relinquish Time after Rising Edge of SCLK
t_8	0	ns min	$\overline{TFS}$ Low to SCLK Falling Edge
	$t_{CLK\ IN}$ + 50	ns max	
t_9	0	ns min	Data Valid to $\overline{TFS}$ Falling Edge Setup Time (A2 Address Bit)
t_{10}	20	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{11}	10	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{12}	20	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
External-Clocking Mode			
t_{13}	20	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{14}[5]	40	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{15}	50	ns min	SCLK High Pulse Width
t_{16}	50	ns min	SCLK Low Pulse Width
t_{17}[5]	35	ns max	SCLK Rising Edge to Data Valid Delay
t_{18}	20	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{19}[6]	50	ns max	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
t_{19A}[6]	90	ns max	Bus Relinquish Time after Rising Edge of SCLK
t_{20}	20	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Setup Time
t_{21}	10	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{22}	15	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{23}	40	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time

NOTES

[1]Sample tested at –25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 8 to 11.

[3]The AD7890 is production tested with $f_{CLK\ IN}$ at 2.5 MHz. It is guaranteed by characterization to operate at 100 kHz.

[4]Specified using 10% and 90% points on waveform of interest.

[5]These numbers are measured with the load circuit of Figure I and defined as the time required for the output to cross 0.8 V or 2.4 V.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

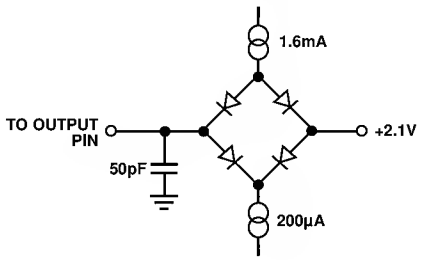


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

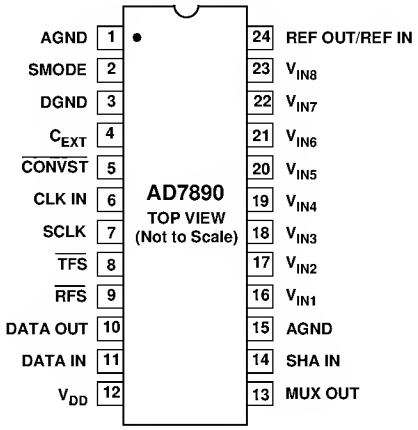
PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
2	SMODE	Control Input. Determines whether the part operates in its External Clocking (slave) or Self-Clocking (master) serial mode. With SMODE at a logic low, the part is in its Self-Clocking serial mode with $\overline{RFS}$ and SCLK as outputs. This Self-Clocking mode is useful for connection to shift registers or to serial ports of DSP processors. With SMODE at a logic high, the part is in its External Clocking serial mode with SCLK and $\overline{RFS}$ as inputs. This External Clocking mode is useful for connection to the serial port of microcontrollers such as the 8XC51 and the 68HCXX and for connection to the serial ports of DSP processors.
3	DGND	Digital Ground. Ground reference for digital circuitry.
4	C_{EXT}	External Capacitor. An external capacitor is connected to this pin to determine the length of the internal pulse (see $\overline{CONVST}$ input and Control Register section). Larger capacitances on this pin extend the pulse to allow for settling time delays through an external antialiasing filter or signal conditioning circuitry.
5	$\overline{CONVST}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion provided that the internal pulse has timed out (see Control Register section). If the internal pulse is active when the $\overline{CONVST}$ goes high, the track/hold will not go into hold until the pulse times out. If the internal pulse has timed out when $\overline{CONVST}$ goes high, the rising edge of $\overline{CONVST}$ drives the track/hold into hold and initiates conversion.
6	CLK IN	Clock Input. An external TTL-compatible clock is applied to this input pin to provide the clock source for the conversion sequence. In the Self-Clocking serial mode, the SCLK output is derived from this CLK IN pin.
7	SCLK	Serial Clock Input. In the External Clocking (slave) mode (see Serial Interface section) this is an externally applied serial clock which is used to load serial data to the control register and to access data from the output register. In the Self-Clocking (master) mode, the internal serial clock, which is derived from the clock input (CLK IN), appears on this pin. Once again, it is used to load serial data to the control register and to access data from the output register.
8	$\overline{TFS}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.
9	$\overline{RFS}$	Receive Frame Synchronization Pulse. In the External Clocking mode, this pin is an active low logic input with $\overline{RFS}$ provided externally as a strobe or framing pulse to access serial data from the output register. In the Self-Clocking mode, it is an active low output which is internally generated and provides a strobe or framing pulse for serial data from the output register. For applications which require that data be transmitted and received at the same time, $\overline{RFS}$ and $\overline{TFS}$ should be connected together.
10	DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with one leading zero, preceding the three address bits of the Control register and the 12 bits of conversion data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding from the ADC is 2s complement for the AD7890-10 and straight binary for the AD7890-4 and AD7890-2.
11	DATA IN	Serial Data Input. Serial data to be loaded to the control register is provided at this input. The first five bits of serial data are loaded to the control register on the first five falling edges of SCLK after $\overline{TFS}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{TFS}$ remains low.
12	V_{DD}	Positive supply voltage, +5 V ± 5%.
13	MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 V to +2.5 V for the nominal analog input range to the selected channel. The output impedance of this output is nominally 3.5 kΩ. If no external antialiasing filter is required, MUX OUT should be connected to SHA IN.
14	SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input and the input voltage range is 0 V to +2.5 V.
15	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
16	V_{IN1}	Analog Input Channel 1. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.

Pin	Mnemonic	Description
17	V_{IN2}	Analog Input Channel 2. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
18	V_{IN3}	Analog Input Channel 3. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
19	V_{IN4}	Analog Input Channel 4. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
20	V_{IN5}	Analog Input Channel 5. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
21	V_{IN6}	Analog Input Channel 6. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
22	V_{IN7}	Analog Input Channel 7. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
23	V_{IN8}	Analog Input Channel 8. Single-ended analog input. The analog input range on is ±10 V (AD7890-10), 0 V to +4.096 V (AD7890-4) and 0 V to +2.5 V (AD7890-2). The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
24	REF OUT/REF IN	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference voltage is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should decoupled to AGND with a 0.1 μF disc ceramic capacitor. The output impedance of this reference source is typically 2 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip. The nominal reference voltage for correct operation of the AD7890 is +2.5 V.

PIN CONFIGURATION

DIP and SOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ \text{dB}$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7890, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7890 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 1 kHz signal to any one of the other seven inputs and determining how much that signal is attenuated in the channel of interest. The figure given is the worst case across all eight channels.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7890-10)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (4 × REF IN – 1 LSB) after the Bipolar Zero Error has been adjusted out.

Positive Full-Scale Error (AD7890-4)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (1.638 × REF IN – 1 LSB) after the Unipolar Offset Error has been adjusted out.

Positive Full-Scale Error (AD7890-2)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (REF IN – 1 LSB) after the Unipolar Offset Error has been adjusted out.

Bipolar Zero Error (AD7890-10)

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal 0 V (AGND).

Unipolar Offset Error (AD7890-2, AD7890-4)

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal 0 V (AGND).

Negative Full-Scale Error (AD7890-10)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (–4 × REF IN + 1 LSB) after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7890. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a channel change/step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CONTROL REGISTER

The Control Register for the AD7890 contains 5 bits of information as described below. Six serial clock pulses must be provided to the part in order to write data to the Control Register (seven if the write is required to put the part in Standby Mode). If $\overline{TFS}$ returns high before six serial clock cycles then no data transfer takes place to the Control Register and the write cycle will have to be restarted to write the data to the Control Register. If, however, the CONV bit of the register (see below) is set to a Logic 1, then a conversion will be initiated whenever a Control Register write takes place regardless of how many serial clock cycles the $\overline{TFS}$ remains low for. The default (power-on) condition of all bits in the Control Register is 0.

MSB

A2	A1	A0	CONV	STBY

A2	Address Input. This input is the most significant address input for multiplexer channel selection.
A1	Address Input. This is the 2nd most significant address input for multiplexer channel selection.
A0	Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal pulse is initiated, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it ensures the conversion process cannot be activated. This allows for the multiplexer settling time and track/hold acquisition time before the track/hold goes into hold and conversion is initiated. In applications where there is an antialiasing filter between MUX OUT and SHA IN, the filter settling time can be taken into account before the input at SHA IN is sampled. When the internal pulse times out, the track/hold goes into hold and conversion is initiated.
CONV	Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{CONVST}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal pulse and the conversion process are initiated after the sixth serial clock cycle of the write operation if a 1 is written to this bit. With a 1 in this bit, the hardware conversion start i.e., the $\overline{CONVST}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{CONVST}$ input.
STBY	Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode. The part does not enter its standby mode until the seventh falling edge of SCLK in a write operation. Therefore, the part requires seven serial clock pulses in its serial write operation if it is required to put the part into standby.

CONVERTER DETAILS

The AD7890 is an eight-channel, 12-bit, single supply, serial data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, reference, A/D converter and versatile serial logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals (AD7890-10) and 0 V to +4.096 V input signals (AD7890-4) while operating from a single +5 V supply. The AD7890-2 contains no signal scaling and accepts an analog input range of 0 V to +2.5 V. The part operates from a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Unlike other single chip data acquisition solutions, the AD7890 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one-chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used on the output of the multiplexer to provide the antialiasing function for all eight channels.

Conversion is initiated on the AD7890 either by pulsing the $\overline{CONVST}$ input or by writing a Logic 1 to the CONV bit of the Control Register. When using the hardware $\overline{CONVST}$ input, on the rising edge of the $\overline{CONVST}$ signal, the on-chip track/hold goes from track to hold mode and the conversion sequence is started provided the internal pulse has timed out. This internal pulse (which appears at the C_{EXT} pin) is initiated whenever the multiplexer address is loaded to the AD7890 Control Register. This pulse goes from high to low when a serial write to the part is initiated. It starts to discharge on the sixth falling clock edge of SCLK in a serial write operation to the part. The track/hold cannot go into hold and conversion cannot be initiated until the C_{EXT} pin has crossed its trigger point of 2.5 V. The discharge time of the voltage on C_{EXT} depends upon the value of capacitor connected to the C_{EXT} pin (see C_{EXT} Functioning section). The fact that the pulse is initiated every time a write to the control register takes place means that the software conversion start and track/hold signal is always delayed by the internal pulse.

The conversion clock for the part is generated from the clock signal applied to the CLK IN pin of the part. Conversion time for the AD7890 is 5.9 μs from the rising edge of the hardware $\overline{CONVST}$ signal and the track/hold acquisition time is 2 μs. To obtain optimum performance from the part, the data read operation or Control Register write operation should not occur during the conversion or during 500 ns prior to the next conversion. This allows the part to operate at throughput rates up to 117 kHz in the external clocking mode and achieve data sheet specifications. The part can operate at slightly higher throughput rates (up to 127 kHz), again in external clocking mode with degraded performance (see Timing and Control section). The throughput rate for self-clocking mode is limited by the serial clock rate to 78 kHz.

All unused inputs should be connected to a voltage within the nominal analog input range to avoid noise pickup. On the AD7890-10, if any one of the input channels which are not being converted goes more negative than –12 V, it can interfere with the conversion on the selected channel.

CIRCUIT DESCRIPTION

Analog Input Section

The AD7890 is offered as three part types, the AD7890-10 which handles a ±10 V input voltage range, the AD7890-4 which handles a 0 V to +4.096 V input range and the AD7890-2 which handles a 0 V to +2.5 V input voltage range.

AD7890-10

Figure 2 shows the analog input section for the AD7890-10. The analog input range for each of the analog inputs is ±10 V into an input resistance of typically 33 kΩ. This input is benign with no dynamic charging currents with the resistor attenuator stage followed by the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs...). Output coding is 2s complement binary with 1 LSB – FS/4096 = 20 V/4096 = 4.88 mV. The ideal input/output transfer function is shown in Table I.

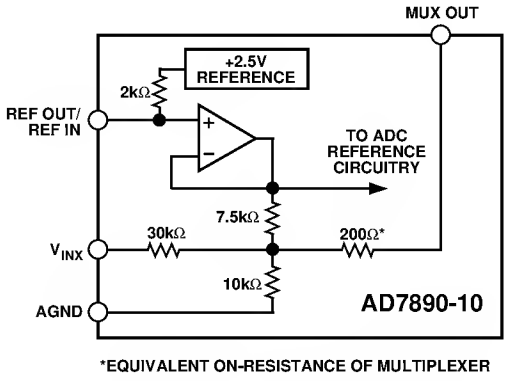


Figure 2. AD7890-10 Analog Input Structure

Table I. Ideal Input/Output Code Table for the AD7890-10

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 1 LSB[2] (9.995117 V)	011 . . . 110 to 011 . . . 111
+FSR/2 – 2 LSBs (9.990234 V)	011 . . . 101 to 011 . . . 110
+FSR/2 – 3 LSBs (9.985352 V)	011 . . . 100 to 011 . . . 101
AGND + 1 LSB (0.004883 V)	000 . . . 000 to 000 . . . 001
AGND (0.000000 V)	111 . . . 111 to 000 . . . 000
AGND – 1 LSB (–0.004883 V)	111 . . . 110 to 111 . . . 111
–FSR/2 + 3 LSBs (–9.985352 V)	100 . . . 010 to 100 . . . 011
–FSR/2 + 2 LSBs (–9.990234 V)	100 . . . 001 to 100 . . . 010
–FSR/2 + 1 LSB (–9.995117 V)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 20 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 4.883 mV with REF IN = +2.5 V.

AD7890-4

Figure 3 shows the analog input section for the AD7890-4. The analog input range for each of the analog inputs is ±10 V into an input resistance of typically 15 kΩ. This input is benign with no dynamic charging currents with the resistor attenuator stage followed by the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is straight (natural) binary with 1 LSB = FS/4096 = 4.096 V/4096 = 1 mV. The ideal input/output transfer function is shown in Table II.

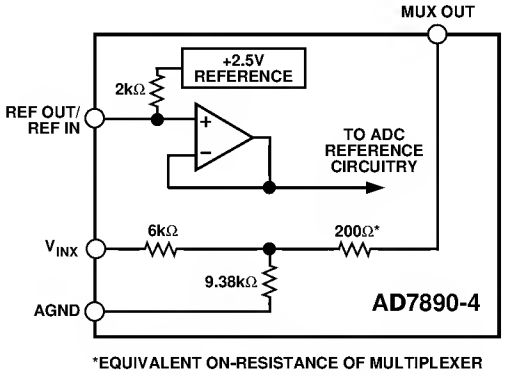


Figure 3. AD7890-4 Analog Input Structure

Table II. Ideal Input/Output Code Table for the AD7890-4

Analog Input[1]	Digital Output Code Transition
+FSR – 1 LSB[2] (4.095 V)	111 . . . 110 to 111 . . . 111
+FSR – 2 LSBs (4.094 V)	111 . . . 101 to 111 . . . 110
+FSR – 3 LSBs (4.093 V)	111 . . . 100 to 111 . . . 101
AGND + 3 LSBs (0.003 V)	000 . . . 010 to 000 . . . 011
AGND + 2 LSBs (0.002 V)	000 . . . 001 to 000 . . . 010
AGND + 1 LSB (0.001 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 4.096 V with REF IN +2.5 V.
[2]1 LSB = FSR/4096 = 1 mV with REF IN = +2.5 V.

AD7890-2

The analog input section for the AD7890-2 contains no biasing resistors and the selected analog input connects to the multiplexer and in cases where MUX OUT is connected to SHA IN this is followed by the high input impedance stage of the track/hold amplifier. The analog input range is, therefore, 0 V to +2.5 V into a high impedance stage with an input current of less than 50 nA. The designed code transitions occur on successive integer LSB values (i.e., l LSB, 2 LSBs, 3 LSBs . . . FS-1 LSBs). Output coding is straight (natural) binary with 1 LSB = FS/4096 = 2.5 V/4096 = 0.61 mV. The ideal input/output transfer function is shown in Table III.

Table III. Ideal Input/Output Code Table for the AD7890-2

Analog Input[1]	Digital Output Code Transition
+FSR – 1 LSB[2] (2.499390 V)	111 . . . 110 to 111 . . . 111
+FSR – 2 LSBs (2.498779 V)	111 . . . 101 to 111 . . . 110
+FSR – 3 LSBs (2.498169 V)	111 . . . 100 to 111 . . . 101
AGND + 3 LSBs (0.001831 V)	000 . . . 010 to 010 . . . 011
AGND + 2 LSBs (0.001221 V)	000 . . . 001 to 001 . . . 010
AGND + 1 LSB (0.000610 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 2.5 V with REF IN = +2.5 V.
[2]1 LSB = FSR/4096 = 0.61 mV with REF IN = +2.5 V.

Track/Hold Section

The SHA IN input on the AD7890 connects directly to the input stage of the track/hold amplifier. This is a high impedance input with input leakage currents of less than 50 nA. Connecting the MUX OUT pin directly to the SHA IN pin connects the multiplexer output directly to the track/hold amplifier. The input voltage range for this input is 0 V to +2.5 V. If external circuitry is connected between MUX OUT and SHA IN, then the user must ensure that the input voltage range to the SHA IN input is 0 V to +2.5 V to ensure that the full dynamic range of the converter is utilized.

The track/hold amplifier on the AD7890 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 117 kHz (i.e., the track/hold can handle input frequencies in excess of 58 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. The start of conversion is the rising edge of $\overline{\text{CONVST}}$ (assuming the internal pulse has timed out) for hardware conversion starts and for software conversion starts is the point where the internal pulse is timed out. The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. For software conversion starts, the time depends on the internal pulse widths. Therefore, for software conversion starts, the sampling instant is not very well defined. For sampling systems which require well defined, equidistant sampling, it may not be possible to achieve optimum performance from the part using the software conversion start. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Section

The AD7890 contains a single reference pin, labelled REF OUT/REF IN, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7890's transfer function and will add to the specified full-scale errors on the part. On the AD7893-10, it will also result in an offset error injected in the attenuator stage.

The AD7890 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7890, simply connect a 0.1 μF disc ceramic capacitor from the REF OUT/REF IN pin to AGND. The voltage which appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7890, it should be buffered as the source impedance of this output is 2 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7890 needs to be used with a system reference, then the user has the option of connecting an external reference to this REF OUT/REF IN pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered but has a nominal 2 kΩ resistor connected to the AD7890's internal reference. Suitable reference sources for the AD7890 include the AD680, AD780 and REF-43 precision +2.5 V references.

Timing and Control Section

The AD7890 is capable of two interface modes, selected by the SMODE input. The first of these is a self-clocking mode where the part provides the frame sync, serial clock and serial data at the end of conversion. In this mode the serial clock rate is determined by the master clock rate of the part (at CLK IN input). The second mode is an external clocking mode where the user provides the frame sync and serial clock signals to obtain the serial data from the part. In this second mode, the user has control of the serial clock rate up to a maximum of 10 MHz. The two modes are discussed in more detail in the Serial Interface section.

The part also provides hardware and software conversion start features. The former provides a well-defined sampling instant with the track/hold going into hold on the rising edge of the $\overline{\text{CONVST}}$ signal. For the software conversion start, a write to the CONV bit to the Control Register initiates the conversion sequence. However, for the software conversion start an internal pulse has to time out before the input signal is sampled. This pulse, plus the difficult in maintaining exactly equal delays between each software conversion start command, means that the dynamic performance of the AD7890 may have difficulty meeting spec when used in software conversion start mode.

The AD7890 provides separate channel select and conversion start control. This allows the user to optimize the throughput rate of the system. Once the track/hold has gone into hold mode, the input channel can be updated and the input voltage can settle to the new value while the present conversion is in progress.

Assuming the internal pulse has timed out before the $\overline{\text{CONVST}}$ pulse is exercised, the conversion will consist of 14.5 master clock cycles. In the self-clocking mode, the conversion time is defined as the time from the rising edge of $\overline{\text{CONVST}}$ to the falling edge of $\overline{\text{RFS}}$ (i.e., when the device starts to transmit its conversion result). This time includes the 14.5 master clock cycles plus the updating of the output register and delay time in outputting the $\overline{\text{RFS}}$ signal, resulting in a total conversion time of 5.9 μs maximum. Figure 4 shows the conversion timing for the AD890 when used in the Self-Clocking (Master) Mode with hardware $\overline{\text{CONVST}}$. The timing diagram assumes that the internal pulse is not active when the $\overline{\text{CONVST}}$ signal goes high. To ensure this, the channel address to be converted should be selected by writing to the Control Register prior to the $\overline{\text{CONVST}}$ pulse. Sufficient setup time should be allowed between the Control Register write and the $\overline{\text{CONVST}}$ to ensure that the internal pulse has timed out. The duration of the internal pulse (and hence the duration of setup time) depends on the value of C_{EXT}.

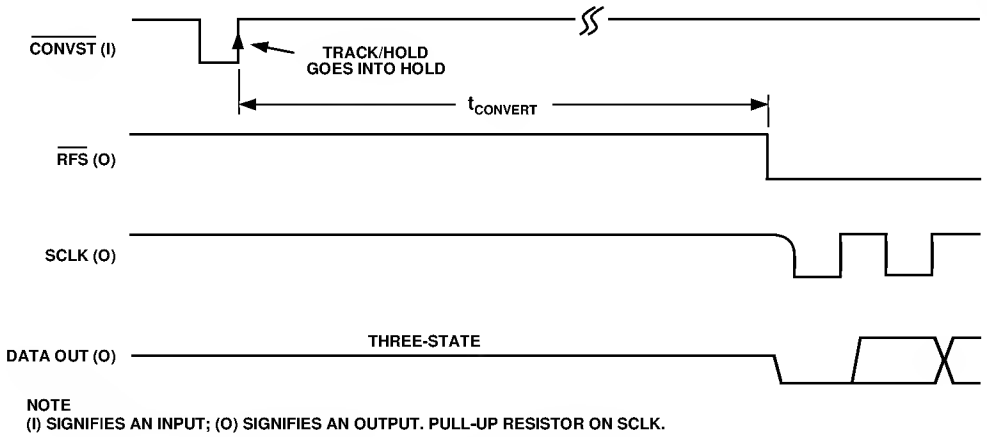


Figure 4. Self-Clocking (Master) Mode Conversion Sequence

When using the device in the External-Clocking Mode, the output register can be read at any time and the most up-to-date conversion result will be obtained. However, reading data from the output register or writing data to the Control Register during conversion or during the 500 ns prior to the next $\overline{\text{CONVST}}$ will result in reduced performance from the part. A read operation to the output register has most effect on performance with the signal-to-noise ratio likely to degrade especially when higher serial clock rates are used while the code flicker from the part will also increase (see AD7890 Performance section).

Figure 5 shows the timing and control sequence required to obtain optimum performance from the part in the external clocking mode. In the sequence shown, conversion is initiated on the rising edge of $\overline{\text{CONVST}}$ and new data is available in the output register of the AD7890 5.9 μs later. Once the read operation has taken place, a further 500 ns should be allowed before the next rising edge of $\overline{\text{CONVST}}$ to optimize the settling of the track/hold before the next conversion is initiated. The diagram shows the read operation and the write operation taking place in parallel. On the sixth falling edge of SCLK in the write sequence the internal pulse will be initiated. Assuming MUX OUT is connected to SHA IN, 2 μs are required between this sixth falling edge of SCLK and the rising edge of $\overline{\text{CONVST}}$ to allow for the full acquisition time of the track/hold amplifier. With the serial clock rate at its maximum of 10 MHz, the achievable throughput rate for the part is 5.9 μs (conversion time) plus 0.6 μs (six serial clock pulses before internal pulse is initiated) plus 2 μs (acquisition time). This results in a minimum throughput time of 8.5 μs (equivalent to a throughput rate of 117 kHz). If the part is operated with a slower serial clock, it will impact the achievable throughput rate for optimum performance.

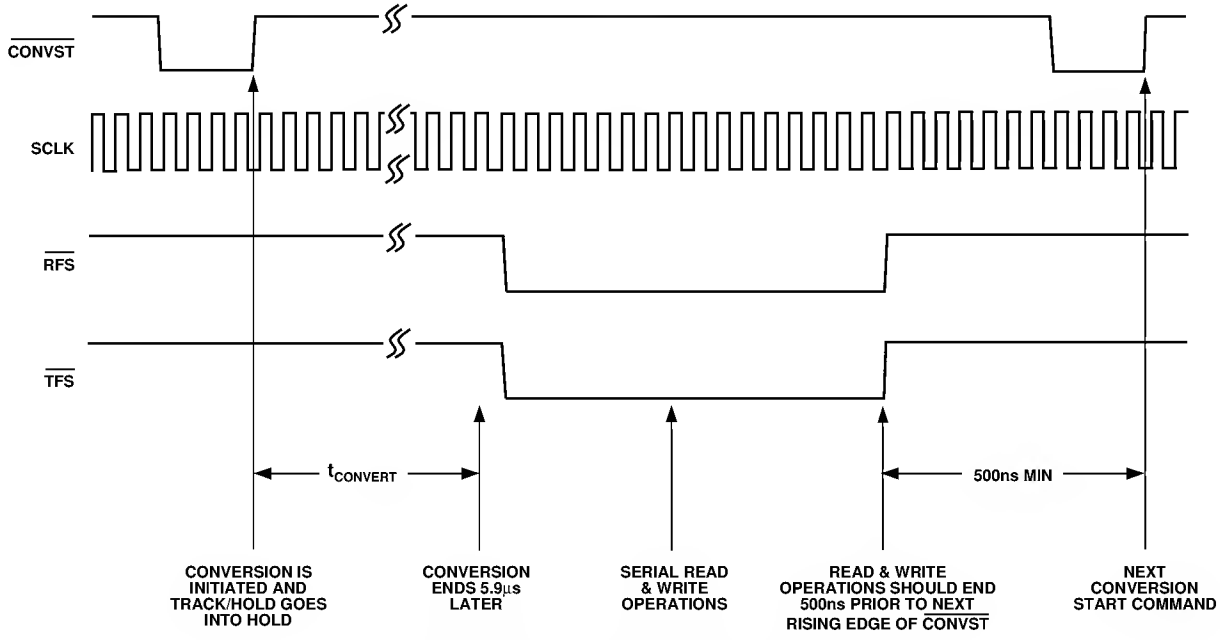


Figure 5. External Clocking (Slave) Mode Timing Sequence for Optimum Performance

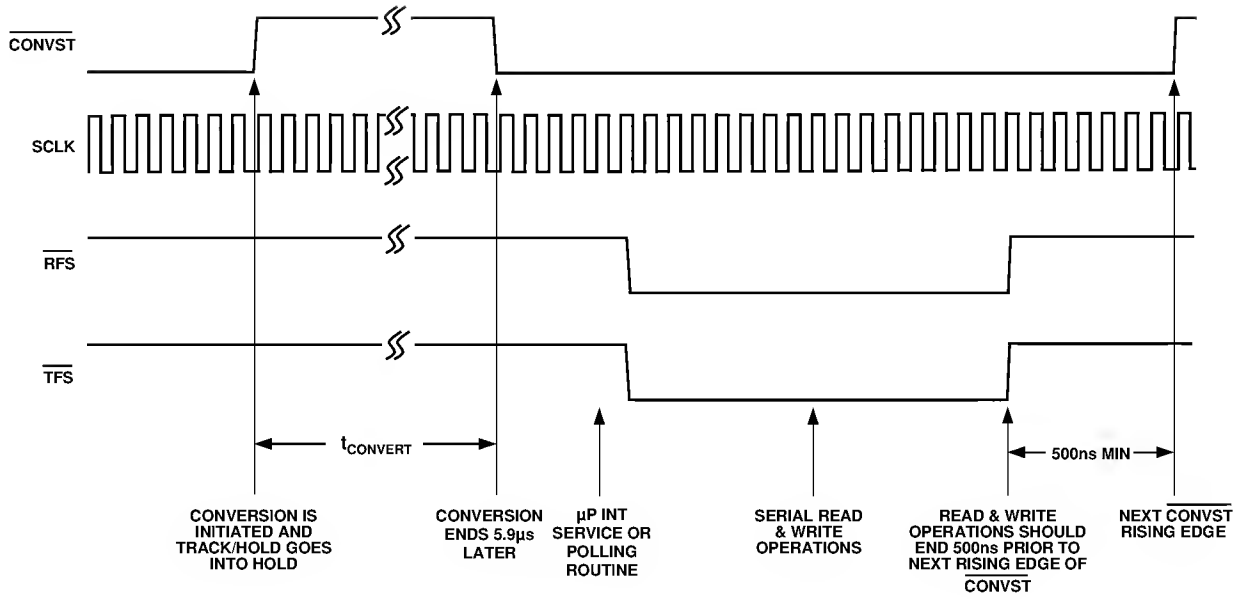


Figure 6. $\overline{CONVST}$ Used as Status Signal in External Clocking Mode

In the Self-Clocking Mode, the AD7890 indicates when conversion is complete by bringing the $\overline{RFS}$ line low and initiating a serial data transfer. In the external clocking mode, there is no indication of when conversion is complete. In many applications, this will not be a problem as the data can be read from the part during conversion or after conversion. However, applications which want to achieve optimum performance from the AD7890 will have to ensure that the data read does not occur during conversion or during 500 ns prior to the rising edge of $\overline{CONVST}$. This can be achieved in either of two ways. The first is to ensure in software that the read operation is not initiated until 5.9 µs after the rising edge of $\overline{CONVST}$. This will only be possible if the software knows when the $\overline{CONVST}$ command is issued. The second scheme would be to use the $\overline{CONVST}$ signal as both the conversion start signal and an interrupt signal. The simplest way to do this would be to generate a square wave signal for $\overline{CONVST}$ with high and low times of 5.9 µs (see Figure 6). Conversion is initiated on the rising edge of $\overline{CONVST}$. The falling edge of $\overline{CONVST}$ occurs 5.9 µs later and can be used as either an active low or falling edge-triggered interrupt signal to tell the processor to read the data from the AD7890. Provided the read operation is completed 500 ns before the rising edge of $\overline{CONVST}$, the AD7890 will operate to specification.

This scheme limits the throughput rate to 11.8 µs minimum. However, depending upon the response time of the microprocessor to the interrupt signal and the time taken by the processor to read the data, this may the fastest which the system could have operated. In any case, the $\overline{CONVST}$ signal does not have to have a 50:50 duty cycle. This can be tailored to optimize the throughput rate of the part for a given system.

Alternatively, the $\overline{CONVST}$ signal can be used as a normal narrow pulse width. The rising edge of $\overline{CONVST}$ can be used as an active high or rising edge-triggered interrupt. A software delay of 5.9 µs can then be implemented before data is read from the part.

C_{EXT} FUNCTIONING

The C_{EXT} input on the AD7890 provides a means of determining how long after a new channel address is written to the part that a conversion can take place. The reason behind this is two-fold. Firstly, when the input channel to the AD7890 is changed, the input voltage on this new channel is likely to be very different from the previous channel voltage. Therefore, the part's track/hold has to acquire the new voltage before an accurate conversion can take place. An internal pulse delays any conversion start command (as well as the signal to send the track/hold into hold) until after this pulse has timed out. The second reason is to allow the user to connect external antialiasing or signal conditioning circuitry between MUX OUT and SHA IN. This external circuitry will introduce extra settling time into the system. The C_{EXT} pin provides a means for the user to extend the internal pulse to take this extra settling time into account. Basically, varying the value of the capacitor on the C_{EXT} pin varies the duration of the internal pulse. Figure 7 shows the relationship between the value of the C_{EXT} capacitor and the internal delay.

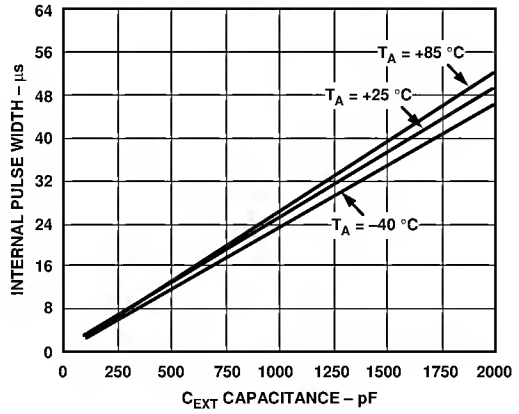


Figure 7. Internal Pulse Width vs. C_{EXT}

The duration of the internal pulse can be seen on the C_{EXT} pin. The C_{EXT} pin goes from a low to a high when a serial write to the part is initiated (on the falling edge of $\overline{TFS}$). It starts to discharge on the sixth falling edge of SCLK in the serial write operation. Once the C_{EXT} pin has discharged to crossing its nominal trigger point of 2.5 V, the internal pulse is timed out.

The internal pulse is initiated each time a write operation to the Control Register takes place. As a result, the pulse is initiated and the conversion process delayed for all software conversion start commands. For hardware conversion start, it is possible to separate the conversion start command from the internal pulse.

If the multiplexer output (MUX OUT) is connected directly to the track/hold input (SHA IN), then no external settling has to be taken into account by the internal pulse width. In applications where the multiplexer is switched and conversion is not initiated until more than 2 μs after the channel is changed (as is possible with a hardware conversion start), the user does not have to worry about connecting any capacitance to the C_{EXT} pin. The 2 μs equates to the track/hold acquisition time of the AD7890. In applications where the multiplexer is switched and conversion is initiated at the same time (such as with a software conversion start), a 120 pF capacitor should be connected to C_{EXT} to allow for the acquisition time of the track/hold before conversion is initiated.

If external circuitry is connected between MUX OUT and SHA IN, then the extra settling time introduced by this circuitry will have to be taken into account. In the case where the multiplexer change command and the conversion start command are separated, they need to be separated by greater than the acquisition time of the AD7890 plus the settling time of the external circuitry if the user does not have to worry about the C_{EXT} capacitance. In applications where the multiplexer is switched and conversion is initiated at the same time (such as with a software conversion start), the capacitor on C_{EXT} needs to allow for the acquisition time of the track/hold plus the settling-time of the external circuitry before conversion is initiated.

SERIAL INTERFACE

The AD7890's serial communications port provides a flexible arrangement to allow easy interfacing to industry-standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7890 accesses data from the output register via the DATA OUT line. A serial write to the AD7890 writes data to the Control Register via the DATA IN line.

Two different modes of operation are available, optimized for different types of interface where the AD7890 can act either as master in the system (it provides the serial clock and data framing signal) or acts as slave (an external serial clock and framing signal can be provided to the AD7890). These two modes, labelled Self-Clocking Mode and External Clocking Mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7890 is configured for its Self-Clocking Mode by tying the SMODE pin of the device to a logic low. In this mode, the AD7890 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7890. This Self-Clocking Mode can be used with processors which allow an external device to clock their serial port including most digital signal processors.

Read Operation

Figure 8 shows a timing diagram for reading from the AD7890 in the Self-Clocking mode. At the end of conversion, $\overline{RFS}$ goes low and the serial clock (SCLK) and serial data (DATA OUT) outputs become active. Sixteen bits of data are transmitted with one leading zero, followed by the three address bits of the Control Register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. The $\overline{RFS}$ output remains low for the duration of the sixteen clock cycles. On the sixteenth rising edge of SCLK, the $\overline{RFS}$ output is driven high and DATA OUT is disabled.

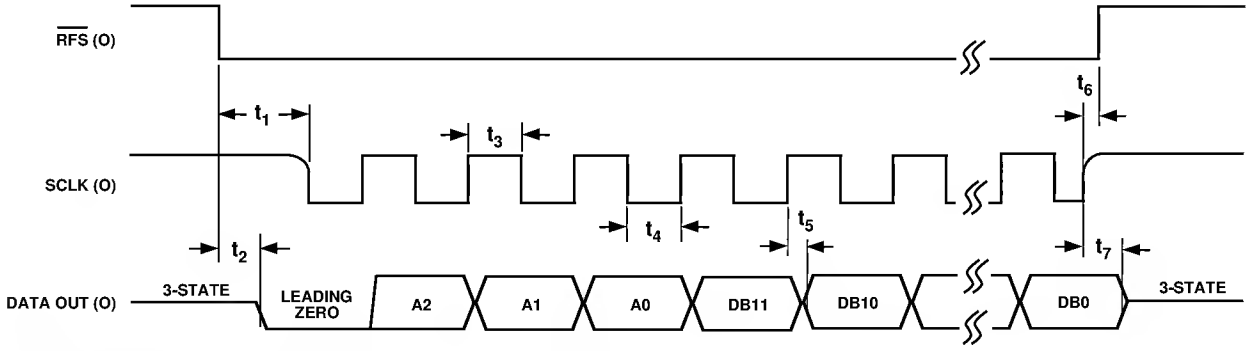


Figure 8. Self-Clocking (Master) Mode Output Register Read

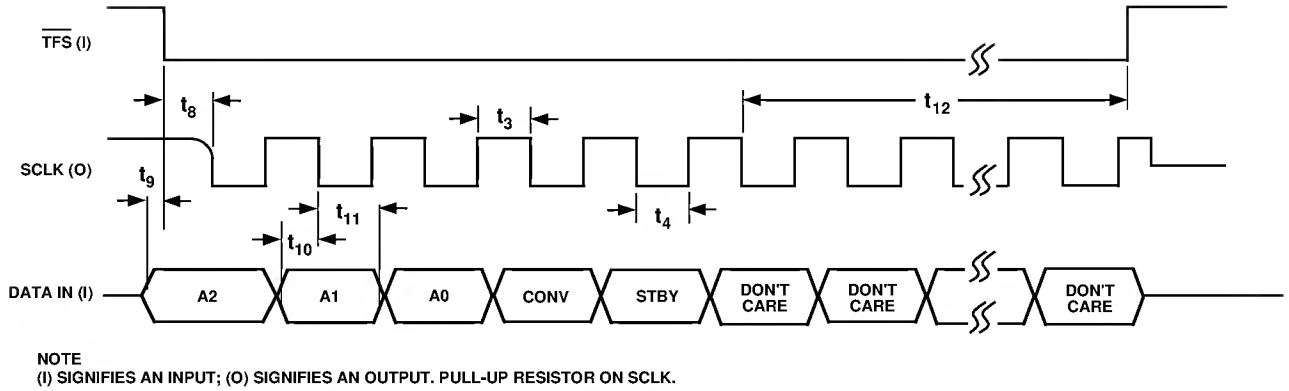


Figure 9. Self-Clocking (Master) Mode Control Register Write

Write Operation

Figure 9 shows a write operation to the Control Register of the AD7890. The $\overline{TFS}$ input is taken low to indicate to the part that a serial write is about to occur. $\overline{TFS}$ going low initiates the SCLK output and this is used to clock data out of the processors serial port and into the Control Register of the AD7890. The AD7890 Control Register requires only five bits of data. These are loaded on the first five clock cycles of the serial clock with data on all subsequent clock cycles being ignored. However, the part requires six serial clock cycles to load data to the Control Register. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

External-Clocking Mode

The AD7890 is configured for its external clocking mode by tying the SMODE pin of the device to a logic high. In this mode, SCLK and $\overline{RFS}$ of the AD7890 are configured as inputs. This external-clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

Figure 10 shows the timing diagram for reading from the AD7890 in the external-clocking mode. $\overline{RFS}$ goes low to access data from the AD7890. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Once again, sixteen bits of data are transmitted with one leading zero, followed by the three address bits in the Control Register, followed by the 12-bit conversion result starting with the MSB. If $\overline{RFS}$ goes low during the high time of SCLK, the leading zero is clocked out from the falling edge of $\overline{RFS}$ (as per Figure 10). If $\overline{RFS}$ goes low during the low time of SCLK, the leading zero is clocked out on the next rising edge of SCLK. This ensures that, regardless of whether $\overline{RFS}$ goes low during a high time or low time of SCLK, the leading zero is valid on the first falling edge of SCLK after $\overline{RFS}$ goes low, provided t_{14} and t_{17} are adhered to. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. At the end of the read operation, the DATA OUT line is three-stated by a rising edge on either the SCLK or $\overline{RFS}$ inputs, whichever occurs first. If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial data read is complete and $\overline{RFS}$ returns high.

Write Operation

Figure 11 shows a write operation to the Control Register of the AD7890. As with the Self-Clocking mode, the $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. As before, the AD7890 Control Register requires only five bits of data. These are loaded on the first five clock cycles of the serial clock with data on all subsequent clock cycles being ignored. However, the part requires six serial clocks to load data to the Control Register. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

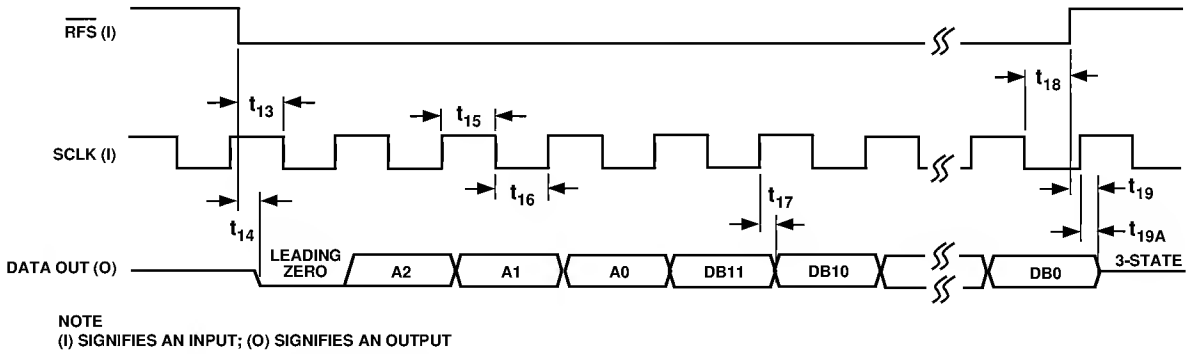


Figure 10. External Clocking (Slave) Mode Output Register Read

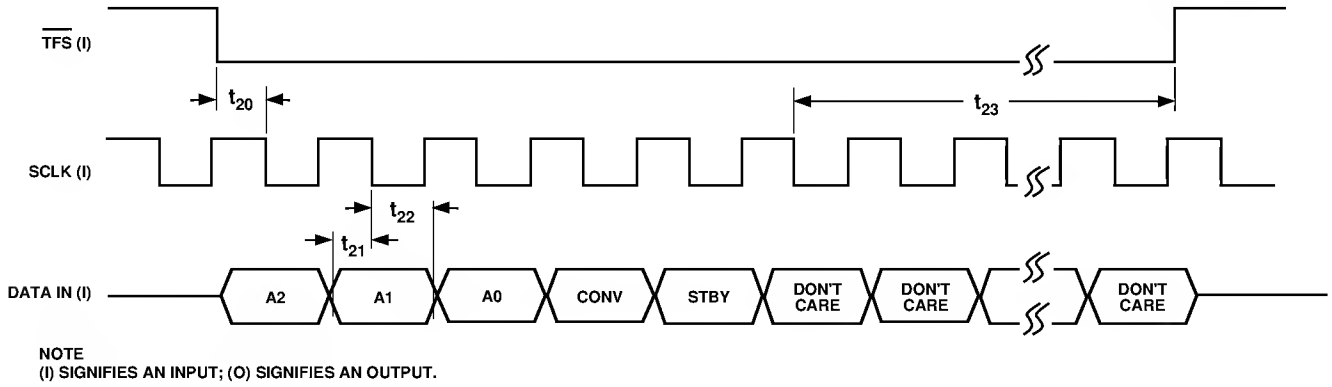


Figure 11. External Clocking (Slave) Mode Control Register Write

SIMPLIFYING THE INTERFACE

To minimize the number of interconnect lines to the AD7890, the user can connect the $\overline{RFS}$ and $\overline{TFS}$ lines of the AD7890 together and read and write from the part simultaneously. In this case, new control register data should be provided on the DATA IN line selecting the input channel and possibly providing a conversion start command while the part provides the result from the conversion just completed on the DATA OUT line.

In the self-clocking mode, this means that the part provides all the signals for the serial interface. It does require that the microprocessor has the data to be written to the Control Register available in its output register when the part brings the $\overline{TFS}$ line low. In the external clocking mode, it means that the user only has to supply a single frame synchronization signal to control both the read and write operations.

Care must be taken with this scheme that the read operation is completed before the next conversion starts if the user wants to obtain optimum performance from the part. In the case of the software conversion start, the conversion command is written to the Control Register on the sixth serial clock edge. However, the read operation continues for another 10 serial clock cycles. To avoid reading during the sampling instant or during conversion, the user should ensure that the internal pulse width is sufficiently long (by choosing C_{EXT}) so that the read operation is completed before the next conversion sequence begins. Failure to do this will result in significantly degraded performance from the part, both in terms of signal-to-noise ratio and dc parameters. In the case of a hardware conversion start, the user should ensure that the delay between the sixth falling edge of the serial clock in the write operation and the next rising edge of $\overline{CONVST}$ is greater than the internal pulse width.

MICROPROCESSOR/MICROCONTROLLER INTERFACE

The AD7890's flexible serial interface allows for easy connection to the serial ports of DSP processors and microcontrollers. Figures 12 through 15 show the AD7890 interfaced to a number of different microcontrollers and DSP processors. In some of the interfaces shown, the AD7890 is configured as the master in the system, providing the serial clock and frame sync for the read operation while in others it acts as a slave with these signals provided by the microprocessor.

AD7890–8051 Interface

Figure 12 shows an interface between the AD7890 and the 8XC51 microcontroller. The AD7890 is configured for its external clocking mode while the 8XC51 is configured for its Mode 0 serial interface mode. The diagram shown in Figure 12 makes no provisions for monitoring when conversion is complete on the AD7890 (assuming hardware conversion start is used). To monitor the conversion time on the AD7890 a scheme such as outlined previously with $\overline{CONVST}$ can be used. This can be implemented in two ways. One is to connect the $\overline{CONVST}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{CONVST}$ line should be connected to the $\overline{INT1}$ input of the 8XC51.

Since the 8XC51 contains only one serial data line, the DATA OUT and DATA IN lines of the AD7890 must be connected together. This means that the 8XC51 cannot communicate with the output register and Control Register of the AD7890 at the same time. The 8XC51 outputs the LSB first in a write operation so care should be taken in arranging the data which is to be transmitted to the AD7890. Similarly, the AD7890 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data that is to be read into the serial port needs to be rearranged before the correct data word from the AD7890 is available in the microcontroller.

The serial clock rate from the 8XC51 is limited to significantly less than the allowable input serial clock frequency with which the AD7890 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7890 cannot run at its maximum throughput rate when used with the 8XC51.

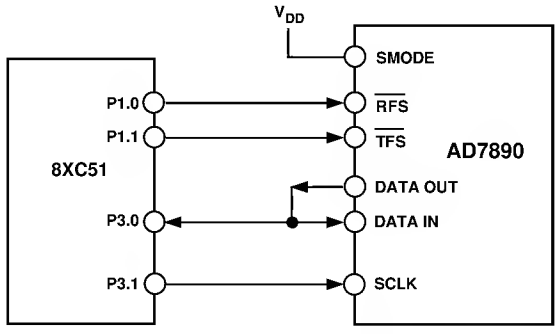


Figure 12. AD7890 to 8XC51 Interface

AD7890–68HC11 Interface

An interface circuit between the AD7890 and the 68HC11 microcontroller is shown in Figure 13. For the interface shown, the AD7890 is configured for its external clocking mode while the 68HC11's SPI port is used and the 68HC11 is configured in its single-chip mode. The 68HC11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one.

As with the previous interface, there are no provisions for monitoring when conversion is complete on the AD7890. To monitor the conversion time on the AD7890 a scheme, such as outlined in the previous interface with $\overline{\text{CONVST}}$, can be used. This can be implemented in two ways. One is to connect the $\overline{\text{CONVST}}$ line to another parallel port bit which is configured as an input. This port bit can then be polled to determine when conversion is complete. An alternative is to use an interrupt driven system in which case the $\overline{\text{CONVST}}$ line should be connected to the $\overline{\text{IRQ}}$ input of the 68HC11.

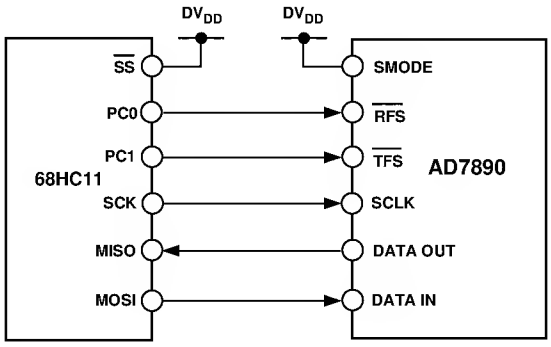


Figure 13. AD7890 to 68HC11 Interface

The serial clock rate from the 68HC11 is limited to significantly less than the allowable input serial clock frequency with which the AD7890 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7890 cannot run at its maximum throughput rate when used with the 68HC11.

AD7890–ADSP-2101 Interface

An interface circuit between the AD7890 and the ADSP-2101 DSP processor is shown in Figure 14. The AD7890 is configured for its external clocking mode with the ADSP-2101 providing the serial clock and frame synchronization signals. The RFS1 and TFS1 inputs are outputs are configured for active low operation.

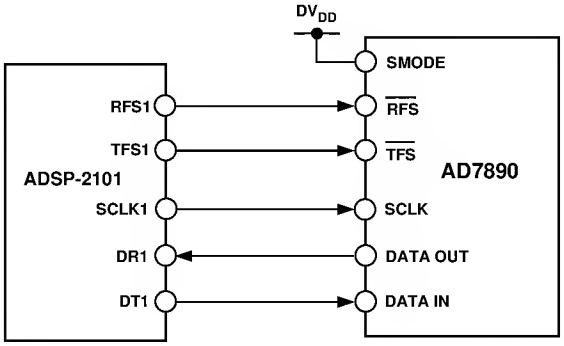


Figure 14. AD7890 to ADSP-2101 Interface

In the scheme shown, the maximum serial clock frequency which the ADSP-2101 can provide is 6.25 MHz. This allows the AD7890 to be operated at a sample rate of 111 kHz. If it is desirable to operate the AD7890 at its maximum throughput rate of 117 kHz, an external serial clock of 10 MHz can be provided to drive the serial clock input of both the AD7890 and the ADSP-2101.

To monitor the conversion time on the AD7890 a scheme, such as outlined in previous interfaces with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQ2}}$ input of the ADSP-2101. An alternative to this, where the user does not have to worry about monitoring the conversion status, is to operate the AD7890 in its Self-Clocking Mode. In this scheme, the actual interface connections would remain the same as in Figure 14 but now the AD7890 provides the serial clock and receive frame synchronization signals. Using the AD7890 in its Self-Clocking Mode, limits the throughput rate of the system as the serial clock rate is limited to 2.5 MHz.

AD7890–DSP56000 Interface

Figure 15 shows an interface circuit between the AD7890 and the DSP56000 DSP processor. The AD7890 is configured for its external clocking mode. The DSP56000 is configured for normal mode, synchronous operation with continuous clock. It is also set up for a 16-bit word with SCK and SC2 as outputs. The FSL bit of the DSP56000 should be set to 0.

The $\overline{\text{RFS}}$ and $\overline{\text{TFS}}$ inputs of the AD7890 are connected together so data is transmitted to and from the AD7890 at the same time. With the DSP56000 in synchronous mode, it provides a common frame synchronization pulse for read and write operations on its SC2 output. This is inverted before being applied to the $\overline{\text{RFS}}$ and $\overline{\text{TFS}}$ inputs of the AD7890.

To monitor the conversion time on the AD7890 a scheme, such as outlined in previous interface examples with $\overline{\text{CONVST}}$, can be used. This can be implemented by connecting the $\overline{\text{CONVST}}$ line directly to the $\overline{\text{IRQA}}$ input of the DSP56000.

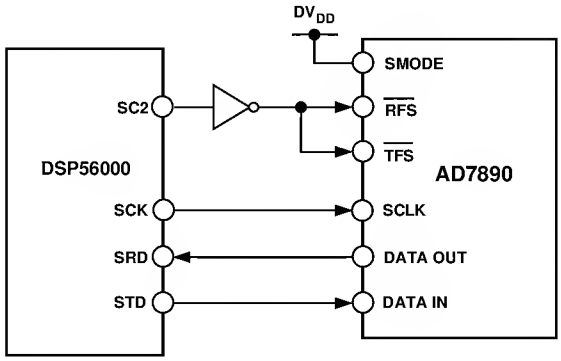


Figure 15. AD7890 to DSP56000 Interface

AD7890–TMS320C25/30 Interface

Figure 16 shows an interface circuit between the AD7890 and the TMS320C25/30 DSP processor. The AD7890 is configured for its Self-Clocking Mode where it provides the serial clock and frame synchronization signals. However, the TMS320C25/30 requires a continuous serial clock. In the scheme outlined here, the AD7890's master clock signal, CLK IN, is used to provide the serial clock for the processor. The AD7890's output SCLK,

to which the serial data is referenced, is a delayed version of the CLK IN signal. The typical delay between the CLK IN and SCLK is 20 ns and will be no more than 50 ns over supplies and temperature. Therefore, there will still be sufficient setup time for DATA OUT to be clocked into the DSP on the edges of the CLK IN signal. When writing data to the AD7890, the processor's data hold time is sufficiently long to cater for the delay between the two clocks. The AD7890's $\overline{RFS}$ signal connects to both the FSX and FSR inputs of the processor. The processor can generate its own FSX signal so if required the interface can be modified so that the $\overline{RFS}$ and $\overline{TFS}$ signals are separated and the processor generates the FSX signal which is connected to the $\overline{TFS}$ input of the AD7890.

In the scheme outlined here, the user does not have to worry about monitoring the end of conversion. Once conversion is complete, the AD7890 takes care of transmitting back its conversion result to the processor. Once the sixteen bits of data have been received by the processor into its serial shift register, it generates an internal interrupt. Since $\overline{RFS}$ and $\overline{TFS}$ are connected together, data is transmitted to the Control Register of the AD7890 whenever the AD7890 transmits its conversion result. The user just has to ensure that the word to be written to the AD7890 Control Register is set up prior to the end of conversion. As part of the interrupt routine which recognizes that data has been read in, the processor can set up the data which it is going to write to the Control Register next time around.

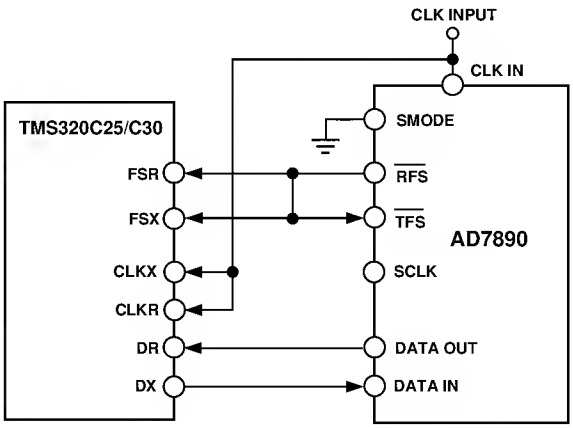


Figure 16. AD7890 to TMS320C25/30 Interface

ANTIALIASING FILTER

The AD7890 provides separate access to the multiplexer and ADC via the MUX OUT and SHA IN pins. One of the reasons for this is to allow the user to implement an antialiasing filter between the multiplexer and the ADC. Inserting the antialiasing filter at this point has the advantage that one antialiasing filter can suffice for all eight channels rather than a separate antialiasing filter for each channel if they were to be placed prior to the multiplexer.

The antialiasing filter inserted between the MUX OUT and SHA IN pins will generally be a low-pass filter to remove high frequency signals which could possibly be aliased back in-band during the sampling process. It is recommended that this filter is an active filter, ideally with the MUX OUT of the AD7890 driving a high impedance stage and the SHA IN of the part being driven from a low impedance stage. This will remove any effects from the variation of the part's multiplexer on-resistance with input signal voltage and will also remove any effects of a high source impedance at the sampling input of the track/hold. With an external antialiasing filter in place, the additional settling-time associated with the filter should be accounted for by using a larger capacitance on C_{EXT}.

AD7890 PERFORMANCE

Linearity

The linearity of the AD7890 is primarily determined by the on-chip 12-bit D/A converter. This is a segmented DAC which is laser trimmed for 12-bit integral linearity and differential linearity. Typical relative numbers for the part are ±1/4 LSB while the typical DNL errors are ±1/2 LSB.

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications. In a sampling A/D converter like the AD7890, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. The input bandwidth of the track/hold exceeds the Nyquist bandwidth and, therefore, an antialiasing filter should be used to remove unwanted signals above $f_S/2$ in the input signal in applications where such signals exist.

Figure 17 shows a histogram plot for 8192 conversions of a dc input using the AD7890. The analog input was set at the centre of a code transition. The timing and control sequence used was as per Figure 5 where the optimum performance of the ADC was achieved. The same performance will be achieved in self-clocking mode where the part transmits its data after conversion is complete. It can be seen that almost all the codes appear in the one output bin indicating very good noise performance from the ADC. The rms noise performance for the AD7890-2 for the above plot was 81 μV. Since the analog input range, and hence LSB size, on the AD7893-4 is 1.638 times what it is for the AD7893-2, the same output code distribution results in an output rms noise of 143 μV for the AD7893-4. For the AD7890-10, with an LSB size eight times that of the AD7890-2, the code distribution represents an output rms noise of 648 μV.

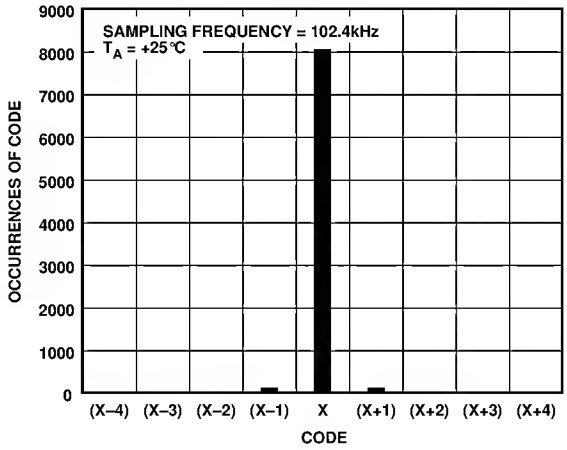


Figure 17. Histogram of 8192 Conversions of a DC Input

In the external clocking mode, it is possible to write data to the Control Register or read data from the output register while a conversion is in progress. The same data is presented in Figure 18 as in Figure 17 except that in this case the output data read for the device occurs during conversion. These results are achieved with a serial clock rate of 2.5 MHz. If a higher serial clock rate is used, the code transition noise will degrade from that shown in the plot of Figure 18. This has the effect of injecting noise onto the die while bit decisions are being made and this increases the noise generated by the AD7890. The histogram plot for 8192 conversions of the same dc input now shows a larger spread of codes with the rms noise for the AD7890-2 increasing to 170 μV. This effect will vary depending on where the serial clock edges appear with respect to the bit trials of the conversion process. It is possible to achieve the same level of performance when reading during conversion as when reading after conversion depending on the relationship of the serial clock edges to the bit trial points (i.e., the relationship of the serial clock edges to the CLK IN edges). The bit decision points on the AD7890 are on the falling edges of the master clock (CLK IN) during the conversion process. Clocking out new data bits at these points (i.e. the rising edge of SCLK) is the most critical from a noise standpoint. The most critical bit decisions are the MSBs, so to achieve the level of performance outlined in Figure 18, reading within 1 μs after the rising edge of $\overline{\text{CONVST}}$ should be avoided.

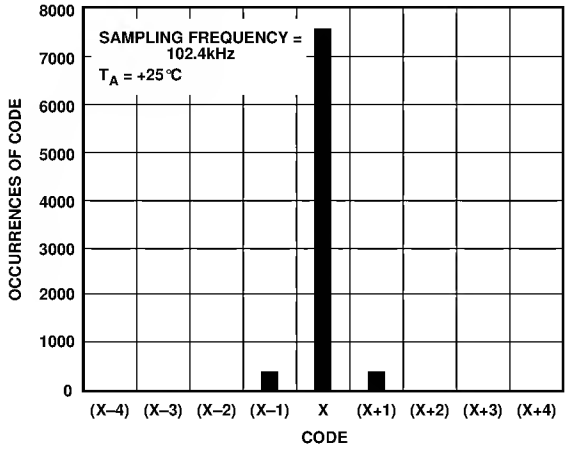


Figure 18. Histogram of 8192 Conversions with Read During Conversion

Writing data to the Control Register also has the effect of introducing digital activity onto the part while conversion is in progress. However, since there are no output drivers active during a write operation, the amount of current flowing on the die is less than for a read operation. Therefore, the amount of noise injected into the die is less than for a read operation. Figure 19 shows the effect of a write operation during conversion. The histogram plot for 8192 conversions of the same dc input now shows a larger spread of codes than for ideal conditions but smaller than for a read operation. The resulting rms noise for the AD7890-2 is 110 μV. In this case, the serial clock frequency was 10 MHz.

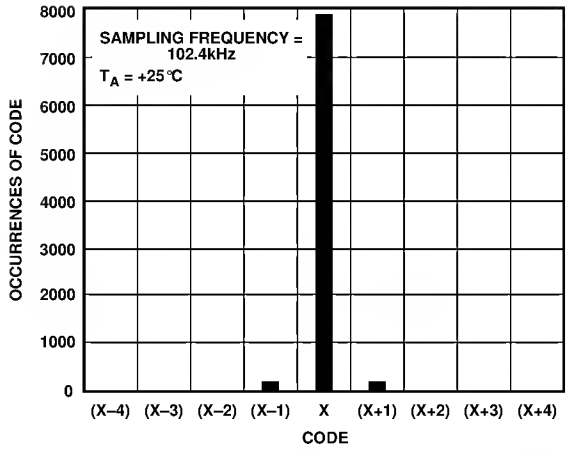


Figure 19. Histogram of 8192 Conversions with Write During Conversion

Dynamic Performance

The AD7890 contains an on-chip track/hold, allowing the part to sample input signals up to 50 kHz on any of its input channels. Many of the AD7890's applications will simply require it to sequence through low frequency input signals across its eight channels. There may be some applications, however, for which the dynamic performance of the converter out to 40 kHz input frequency is of interest. It is recommended for these wider band sampling applications that the hardware conversion start method is used for reasons outlined previously.

These applications require information on the ADC's effect on the spectral content of the input signal. Signal to (Noise + Distortion), total harmonic distortion, peak harmonic or spurious and intermodulation distortion are all specified. Figure 20 shows a typical FFT plot of a 10 kHz, 0 V to +2.5 V input after being digitized by the AD7890-2 operating at a 102.4 kHz sampling rate. The signal to (Noise + Distortion) is 71.5 dB and the total harmonic distortion is –85 dB. It should be noted that reading data from the part during conversion at 10 MHz serial clock does have a significant impact on dynamic performance. Therefore, for sampling applications, it is recommended not to read data during conversion.

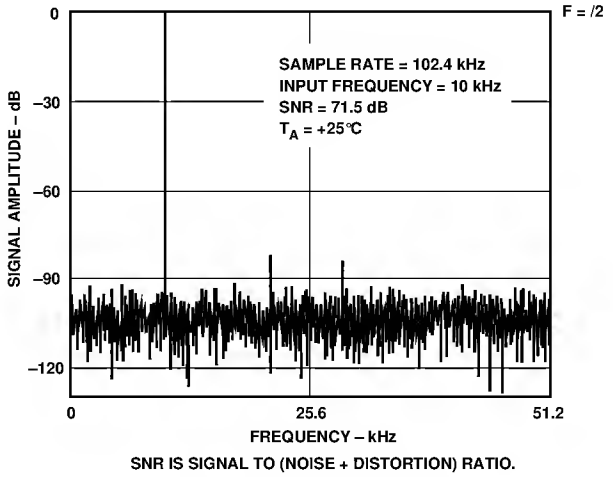


Figure 20. AD7890 FFT Plot

Effective Number of Bits

The formula for Signal to (Noise + Distortion) Ratio (See Terminology section) is related to the resolution or number of bits in the converter. Rewriting the formula, below, gives a measure of performance expressed in effective number of bits (N):

$$N = (SNR - 1.76)/6.02$$

where SNR is Signal to (Noise + Distortion) Ratio

The effective number of bits for a device can be calculated from its measured Signal to (Noise + Distortion) Ratio. Figure 21 shows a typical plot of effective number of bits versus frequency for the AD7890-2 from dc to 40 kHz. The sampling frequency is 102.4 kHz. The plot shows that the AD7890 converts an input sine wave of 40 kHz to an effective numbers of bits of 11 which equates to a Signal to (Noise + Distortion) level of 68 dB.

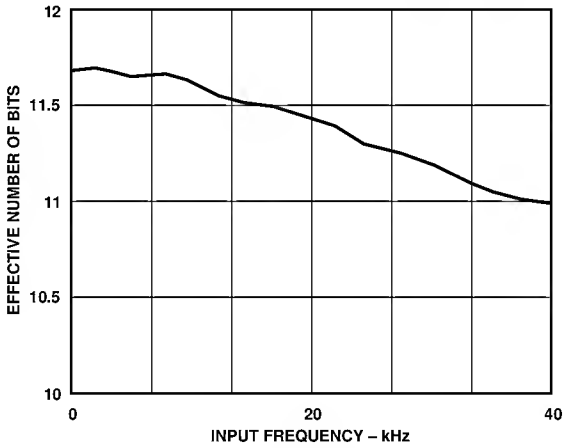
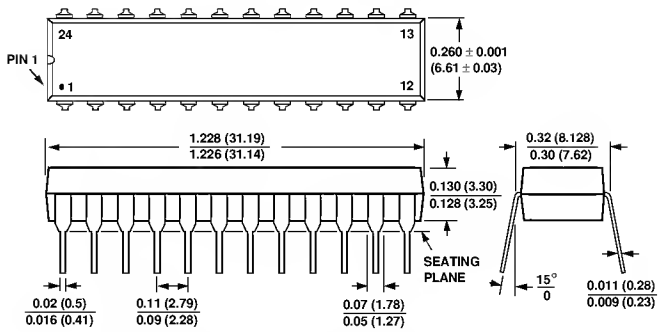


Figure 21. Effective Number of Bits vs. Frequency

OUTLINE DIMENSIONS

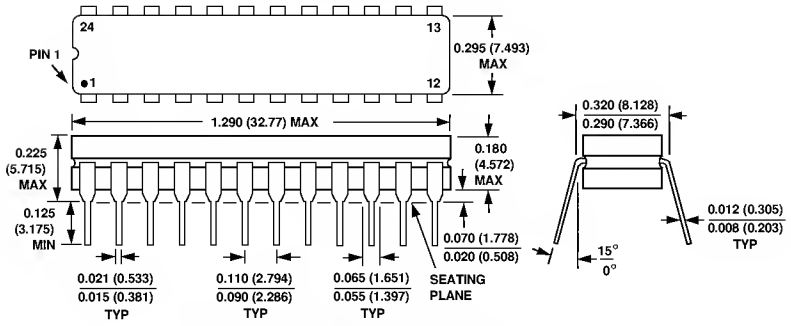
Dimensions shown in inches and (mm).

Plastic DIP (N-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

Cerdip (Q-24)



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

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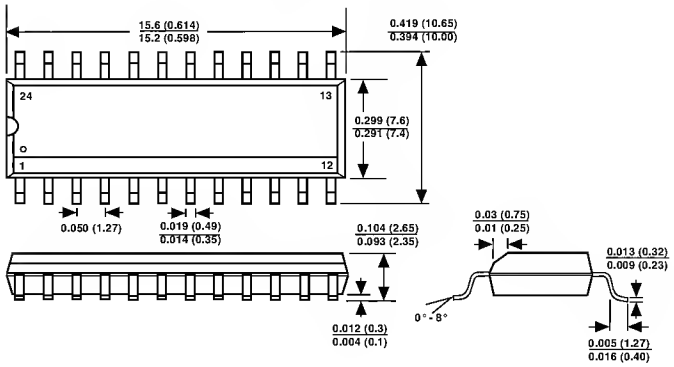

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